REMARKS

Claims 1-20 are pending. Claims 1-20 are rejected. The specification is objected to. The drawings are objected to. The specification has been amended. Formal drawings have been submitted. Claims 1, 3, 4, 5, 8, 17, and 18 have been amended. No new matter has been added.

Objection to the Specification

The specification was objected to because of an informality appearing therein. Applicants assert that this informality has been remedied, based on the present amendment to the specification. The Applicants request that this objection be withdrawn.

Objection to the Drawings

The drawings were objected to because of informalities appearing therein. New corrected drawings in compliance with 37 CFR 1.121(d) accompany this response. Applicants assert that these informalities have been remedied, and request that this objection be withdrawn.

35 U.S.C. 112 ¶ 2 Rejections

Claim 1 is rejected under 35 U.S.C. 112 ¶ 2 as being indefinite. Claim 1 has been amended. Applicant respectfully asserts that Claim 1 as amended overcomes the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claims 2 and 16 are rejected under 35 U.S.C. 112 ¶ 2 as being indefinite, for reciting the term "POD" without first defining the term. Applicant respectfully disagrees. Applicant submits that a POD, within the context of in circuit emulation (ICE), is a term well-known to one having ordinary skill in the art. Therefore, Claims 2 and 16 overcome the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claims 3 and 17 are rejected under 35 U.S.C. 112 ¶ 2 for the inclusion of a relative term, not defined in the claims or specification. Claims 3 and 17 have been amended. Applicant respectfully asserts that Claims 3 and 17 as amended overcome the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claim 4 is rejected under 35 U.S.C. 112 ¶ 2 as being indefinite, for the inclusion of an acronym without first defining the acronym. Claim 4 has been amended. Applicant respectfully asserts that Claim 4 as amended overcomes the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claims 5 and 18 are rejected under 35 U.S.C. 112 ¶ 2 as being indefinite. Claims 5 and 18 have been amended. Applicant respectfully asserts that Claims 5 and 18 as amended overcome the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claim 8 is rejected under 35 U.S.C. 112 ¶ 2 as being indefinite. Claim 8 has been amended. Applicant respectfully asserts that Claim 8 as amended overcomes the basis for rejection under 35 U.S.C. 112 ¶ 2.

Claim 10 is rejected under 35 U.S.C. 112 ¶ 2 as being indefinite, for the inclusion of "locating an error." The rejection suggests that Claim 10 recites a step that produces no result, that Claim 10 recites a step that requires human cognition, and that the definition of "an error" is required. Applicant respectfully disagrees.

The examiner is respectfully directed to dependent Claim 10, which recites that an embodiment of the present invention is directed to:

> The method of Claim 9 further comprising:
> locating an error within the microcontroller test code by tracing the execution history using the trace buffer.

The step recited in Claim 10 produces a result, in that it locates an error within the microcontroller test code; this result is achieved by tracing the execution history using the trace buffer, as claimed. Further, Applicant submits that Claim 10 does not recite a step that requires human cognition. Finally, Applicant respectfully asserts that the meaning of the term "an error," in the context of in circuit emulation, would be well-known to one having ordinary skill in the art. Applicant respectfully contends that Claim 10 overcomes the basis for rejection under 35 U.S.C. 112 ¶ 2.

35 U.S.C. 103(a) Rejections

Claims 1-2, 4-11, 13-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being obvious over Profit, U.S. Patent No. 5,911,059.

The Examiner is respectfully directed to independent Claim 1, which recites that an embodiment of the present invention is directed to:

> A system for debugging microcontroller code comprising:
> a microcontroller installed on a test circuit, wherein the microcontroller includes a first memory and a first CPU;
> an ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system, wherein the ICE emulates the microcontroller, the microcontroller and the ICE run the microcontroller code in lock step; and
> an interface for coupling the test circuit and the ICE enabling data transmission between the test circuit and the computer system, the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step.

Claims 9 and 15 recite similar limitations. Claims 2 and 4-9 are dependent upon Claim 1, and recite additional features of the claimed invention. Claims 10-11, 13, and 14 are dependent upon Claim 9, and recite additional features of the claimed invention. Claims 16 and 18-20 are dependent upon Claim 15, and recite additional features of the claimed invention.

The rejection suggests that Profit discloses every element of Claim 1 to such an extent that it would be obvious to one having ordinary skill in the art to adapt the device described in Profit to achieve the embodiments of the present invention recited in Claim 1. Applicant has reviewed Profit, and respectfully disagrees. Applicant contends that Profit fails to disclose an ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system, as claimed. Applicant further contends that Profit fails to disclose the ICE emulating the microcontroller, as claimed. Applicant also contends that Profit fails to disclose the ICE and the microcontroller running the microcontroller code in lock step, as claimed.

The rejection suggests that Profit discloses an ICE including a second memory and second CPU coupled to a computer system, as claimed. However, the portion of Profit offered to show this element describes a hardware simulator running on a host computer, see col. 5, ln. 63-67. Profit explains that this hardware simulator is used to emulate the target *circuitry*, which is the external circuitry that interacts with the target microprocessor, see col. 1, ln. 20-24. The hardware simulator of Profit is not an in circuit emulator.

The rejection further suggests that Profit discloses the ICE emulating the microcontroller, as claimed. However, the portion of Profit offered to show this element is describing the function of the hardware simulator described above. Profit describes the hardware simulator as being a conventional software program that simulates the electrical and logical activity of the *target circuitry* as seen by the target processor; see col. 6, ln. 25-29. From the example provided, the hardware simulator of Profit is principally a processor model shell, which simulates activity at the target processor's pins; it does not emulate the processor's functionality, see col. 6, ln. 25-48.

The rejection also suggests that Profit discloses the ICE and the microcontroller running the microcontroller code in lock step, as claimed. However, the portions of Profit offered to show this element do not show lock step running of the microcontroller code. First, the functionality of the hardware simulator is referenced. The example

provided by Profit of interaction between the target microcontroller and the hardware simulator does not suggest running the microcontroller code on both; rather, the hardware simulator receives instructions from the microcontroller to execute certain behaviors, and converts interrupts and other events into processor functions that allow the target program executing in the processor emulator to handle the interrupt or event; see col. 6, ln. 25-47. The second portion of Profit referenced describes the operation of the simulation time keeper circuit, which may serve as a clock to keep the processor emulator and the hardware emulator running synchronously; see col. 10, ln. 32. through col. 11, ln. 43. However, as noted previously, the hardware simulator emulates the operation of the target circuitry; it is not an ICE, as claimed.

Therefore, Profit does not anticipate or render obvious the embodiments of the present invention recited in Claims 1, 9, and 15. Applicant respectfully submits that Claims 1, 9, and 15 overcome the basis for rejection under 35 U.S.C. 103(a), and are in condition for allowance. Accordingly, Applicant respectfully submits that Claims 2 and 4-9, dependent on Claim 1, Claims 10-11 and 13-14, dependent on Claim 9, and Claims 16 and 18-20, dependent on Claim 15, overcome the basis for rejection under 35 U.S.C. 103(a), as they are dependent on allowable base claims.

Claims 3, 12, and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Profit in view of Barnett, U.S. Patent No. 6,173,419 B1. Applicant respectfully disagrees.

Barnett does not overcome the deficiencies of Profit. Barnett does not disclose an ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system, as claimed. Nor does Barnett disclose the ICE emulating the microcontroller, as claimed. Barnett further fails to disclose the ICE and the microcontroller running the microcontroller code in lock step, as claimed. Therefore, Profit, alone or in combination with Barnett, does not anticipate or render obvious the embodiments of the present invention recited in Claims 3, 12, and 17. Applicant respectfully submits that Claims 3, 12, and 17 overcome the basis for rejection under 35 U.S.C. 103(a), and are in condition for allowance.

Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: 9/1, 2005

Kevin A. Brown
Reg. No. 56,303
Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060